IN THE CLAIMS

Claims 1-58 (Canceled)

59. (Previously Presented) A signal generating circuit comprising:

a first generating means for generating a first periodic signal;

a second generating means for generating a second periodic signal which is in anti-phase with the first periodic signal;

a frequency divider circuit comprising,

(i) first and second input terminals for respectively receiving the first and second periodic signals;

(ii) an even number of amplifier stages connected in series with an output of the last amplifier stage being connected to an input of the first amplifier stage, wherein each amplifier stage has an associated propagation delay and a transistor coupled between a supply terminal and a reference terminal for modulating the propagation delay through the associated amplifier stage;

(iii) means for applying said first periodic signal received at said first input terminal to a control electrode of said transistor of the or each odd amplifier stage and for applying said second periodic signal received at said second input terminal to a control electrode of said transistor of the or each even amplifier stage, to modulate the propagation delays through the associated amplifier stages about half the period of said first and second periodic signals so that when the propagation delay through the or each even amplifier stage decreases, the propagation delay through the or each odd amplifier stage increases; and

(iv) an output terminal connected to the output of said last amplifier stage for outputting a generated frequency divided signal;

wherein said first and second generating means are arranged to generate the respective first and second periodic signals as analogue periodic signals having an amplitude which causes said transistors to be not fully open or fully closed but to act as variable resistances.

60. (Previously Presented) A circuit according to claim 59, wherein there are two amplifier stages connected in series.

61. (Previously Presented) A circuit according to claim 59, comprising a plurality of said frequency divider circuits connected in series.

62. (Previously Presented) A circuit according to claim 59, wherein each amplifier stage comprises a differential amplifier.

63. (Previously Presented) A circuit according to claim 59, wherein each amplifier stage comprises connection logic circuitry which includes said transistor so that for each amplifier stage the respective one of the first and second analogue periodic signals is operable to vary the propagation delay through the connection logic circuitry.

64. (Previously Presented) A circuit according to claim 59, wherein each amplifier stage comprises an amplifier with hysteresis which includes said transistor so that for each amplifier stage the respective one of the first and second periodic signals is operable to vary the hysteresis of the respective amplifier.

65. (Previously Presented) A circuit according to claim 59, wherein said frequency divider circuit is a FET type semiconductor circuit.

66. (Previously Presented) A circuit according to claim 65, wherein said frequency divider circuit is integrated monolithically with complementary FET logic.

67. (Previously Presented) A circuit according to claim 65, wherein said frequency divider circuit is a CMOS circuit integrated monolithically with CMOS logic circuitry.

68. (Previously Presented) A circuit according to claim 65, wherein said transistor is a first transistor, and wherein the input to each amplifier stage is formed by the gate of a second transistor.

69. (Previously Presented) A circuit according to claim 68, wherein the first and second transistors are connected in series between the supply terminal and the reference terminal.

70. (Previously Presented) A circuit according to claim 59, wherein the first and second analogue periodic signals have a frequency greater than 100 MHz.

71. (Previously Presented) A circuit according to claim 59, wherein said frequency divider circuit further comprises logic means for providing dividing by ratios other than simple powers of two.

72. (Previously Presented) A circuit according to claim 59, wherein each of said amplifier stages comprises a latch circuit having two inverters connected in a memory arrangement with the output of one connected to the input of the other.

73. (Previously Presented) A circuit according to claim 72 in which each inverter comprises a p-channel transistor and a n-channel transistor, and wherein the latch circuit further comprises two pairs of n-channel transistors operable to control the state of said memory arrangement.

74. (Previously Presented) A circuit according to claim 73, wherein the aspect ratio of the n-channel transistor of each inverter is less than the aspect ratio of the n-channel transistors in the two pairs of n-channel transistors which control the state of said memory arrangement.

75. (Previously Presented) A method of frequency division using an even number of amplifier stages connected in series, with an output of the last amplifier stage connected to an input of the first amplifier stage and each amplifier stage having a transistor coupled between a supply terminal and a reference terminal, said method comprising the steps of:

applying a first periodic signal to be frequency divided by the frequency divider circuit to a control electrode of the respective transistor of the or each odd amplifier stage; and

applying a second periodic signal which is in anti-phase with the first periodic signal to a control electrode of the respective transistor of the or each even amplifier stage,

thereby to modulate the propagation delays through the associated amplifier stages about half the period of said first and second periodic signals so that when the propagation delay through the or each even amplifier stage decreases, the propagation delay through the or each odd amplifier stage increases, to generate frequency divided signal at the output of said last amplifier stage;

wherein said applying steps apply analogue periodic signals to said control electrodes, which analogue periodic signals have an amplitude which cause said transistors to not fully open or fully close but to act as a variable resistances.

76. (Previously Presented) A method according to claim 75, wherein each amplifier stage used comprises a differential amplifier.

77. (Previously Presented) A method according to claim 75, wherein each amplifier stage used comprises an amplifier with hysteresis.

78. (Previously Presented) A method according to claim 75, wherein applying the first and second periodic signals varies the strength of connection between adjacent amplifier stages.

79. (Previously Presented) A method according to claim 77, wherein applying the first and second periodic signals varies the hysteresis of each of said amplifier stages.

80. (Previously Presented) A method according to claim 75, wherein said amplifier stages used comprise an FET type semiconductor integrated circuit.

81. (Previously Presented) A method according to claim 80, wherein said amplifier stages used comprise a CMOS integrated circuit.

82. (Previously Presented) A method according to claim 75, wherein the frequency of the input signal to be divided is greater than 100 MHz.

83. (Previously Presented) A method according to claim 75, wherein said method also uses logic circuits for providing division by ratios other than simple powers of two.

84. (Previously Presented) A radio receiver comprising:

a first generating means for generating a first periodic signal;

a second generating means for generating a second periodic signal which is in anti-phase with the first periodic signal;

a frequency divider circuit comprising,

(i) first and second input terminals for respectively receiving the first and second periodic signals;

(ii) an even number of amplifier stages connected in series with an output of the last amplifier stage being connected to an input of the first amplifier stage, wherein each amplifier stage has an associated propagation delay and a transistor coupled between a supply terminal and a reference terminal for modulating the propagation delay through the associated amplifier stage;

(iii) means for applying said first periodic signal received at said first input terminal to a control electrode of said transistor of the or each odd amplifier stage and for applying said second periodic signal received at said second input terminal to a control electrode of said transistor of the or each even amplifier stage, to modulate the propagation delays through the associated amplifier stages about half the period of said first and second periodic signals so that when the propagation delay through the or each even amplifier stage decreases, the propagation delay through the or each odd amplifier stage increases; and

(iv) an output terminal connected to the output of said last amplifier stage for outputting a generated frequency divided signal;

wherein said first and second generating means are arranged to generate the respective first and second periodic signals as analogue periodic signals having an amplitude which causes said transistors to be not fully open or fully closed but to act as variable resistances.

CONCLUSION

Applicant respectfully submits that the claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney ((612) 349-9592) to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743

Respectfully submitted,

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